unmapped with respect to the active pixel area (e.g., active area **314.16**, **314.17**, **314.18**, **314.20**; FIGS. **16**, **17**, **18**, **20**, respectively) for border pixel information stored therein.

In step **2120**, the HAL determines a color for pixels constituting the border (e.g., border pixels **312**; FIGS. **16**B, **17**B, **18**B, **19**B) surrounding an active screen area (e.g., active area **314.16**, **314.16**, **314.17**, **314.18**; FIGS. **16**B, **17**B, **18**B, **19**B), itself under the control under the exclusive control of an OS (e.g., OS **1010**; FIGS. **15**, **19**). The HAL generates a pixel border color signal corresponding to the color determined for the border pixels.

In step **2130**, it is determined whether the HAL will require external (synchronization to transfer border pixel data for display upon the pixels constituting the border, or whether the HAL will perform such synchronization internally.

If it is determined (step **2130**) that no such synchronization external to the HAL is required, e.g., wherein the HAL performs any required synchronization internally, process **2100** proceeds via step **2140**, wherein the HAL transfers border pixel data, in the form of the border pixel color signal, via an LCD controller (e.g., LCD controller **322**; FIG. **19**) directly to LCD drivers (e.g., LCD drivers **326** (**410**), **326**(**422**); FIG. **19**).

If it is determined (step **2130**) that synchronization external to the HAL is required, process **2100** proceeds via step **2145**, wherein the HAL transfers border pixel data, in the form of the border pixel color signal, via an LCD controller (e.g., LCD controller **322**; FIG. **19**) to a timing generator, such as a timing ASIC (e.g., ASIC **324.15**; FIG. **15**).

The ASIC or other timing generator synchronizes the data with the visual information formatted by the OS (e.g., for control of the active area information display), generates a corresponding border pixel color writing signal, and transfers the data, in the form of the border pixel color writing signal, to the LCD drivers; step **2146**.

In the event that the HAL performed any requisite synchronization internally, the border pixel color writing signal is generated by the LCD controller in response to the HAL transferring a border pixel color signal to the LCD controller (step **2140**).

Whether the border pixel color writing signal is generated by the LCD driver in direct response to the HAL transferring a border pixel color signal (step **2140**), or whether the border pixel color writing signal is generated by the ASIC or other timing mechanism, external to the HAL (step **2146**), the LCD drivers are impelled by the border pixel color writing signal to write color data to the border pixels (e.g., border pixels **312**; FIGS. **16**B, **17**B, **18**B, **19**B) accordingly; step **2150**. Process **2100** is complete at this point.

In summary, a display unit is constituted in one embodiment herein by a passive matrix of independently controllable pixels characterized by an active area of n rows and m columns of discrete pixels and a pixel border. In one embodiment, m and n are both 160. The passive matrix is operable to generate an image in response to electronic signals driven from row and column drivers coupled to it, representative of information stored in a frame buffer memory. The pixel border has a predetermined width, and surrounds the passive matrix active area. In one embodiment, the predetermined width is two pixels. The border pixel color state is controlled herein by the frame buffer memory. The pixel border color state is controlled to correspond to information contained in a locus of the frame buffer memory. This locus may be, in various embodiments herein, a single pixel, a row of pixels, or a number of rows of pixels of frame buffer memory. Each row of pixels may be equal to m and/or n, and may be 160. In one embodiment, the frame buffer controls the border pixels directly via a liquid crystal display controller and drivers, without a timing generation mechanism, such as a timing ASIC. In one embodiment, the display unit constitutes a part of a portable electronic device.

In one embodiment, a method of controlling the color of the border pixels constitutes a process including monitoring a locus within the frame buffer memory for information, determining a color for the border pixels corresponding thereto, generating a pixel border color signal corresponding to the color, transferring the pixel border color signal to the liquid crystal display controller, which generates a pixel border color writing signal and impels the drivers to write a color to the border pixels accordingly. The hardware abstraction layer monitors the frame buffer memory locus, determines the border pixel color, and generates the pixel border color signal. In one embodiment, impelling the drivers to write a color to the pixel border does not involve a timing synchronization mechanism external from the hardware abstraction layer.

The preferred embodiment of the present invention, an apparatus and method for achieving a controllable, variable color pixel border for a negative display mode display screen with a passive matrix drive, is thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

What is claimed is:

1. A display unit comprising:

a display passive matrix of independently controllable pixels comprising n rows and m columns of discrete pixels, said display matrix operable to generate an image in response to electronic signals driven from row and column drivers coupled thereto, said image representative of information stored in a frame buffer memory of a hardware abstraction layer; and

a pixel border surrounding said display matrix and comprising a plurality of pixels which are controlled to a color state by one or more unmapped locations of said frame buffer memory without a timing synchronization mechanism external from said hardware abstraction layer.

2. A display unit as described in claim **1** wherein said color state of said pixel border is controlled to correspond to information within a locus of said frame buffer, said locus comprising one or more unmapped memory locations within said frame buffer memory.

3. A display unit as described in claim **2** wherein said locus of said frame buffer comprises a single pixel of memory within said frame buffer.

4. (Original) A display unit as described in claim **2** wherein said locus of said frame buffer comprises a row of pixels of memory within said frame buffer.

5. A display unit as described in claim **4** wherein said row of pixels of memory within said frame buffer comprises n pixels of memory within said frame buffer.

6. A display unit as described in claim **2** wherein said locus of said frame buffer comprises a plurality of rows of pixels of memory within said frame buffer.

7. A display unit as described in claim **6** wherein each said row of pixels of memory within said frame buffer comprises n pixels of memory within said frame buffer, each said row mapping to a corresponding portion of said plurality of pixels comprising said pixel border.